IN THE CLAIMS

Please cancel Claims 9 and 24 without prejudice or disclaimer.

Claims 1 and 2 (cancelled)

Claim 3 (previously amended): A data communication device for communicating data with a peripheral device, the data communication device comprising:

a central processing unit;

a bus interface in communication with the central processing unit, the bus interface comprising a receiver;

at least one peripheral device;

a receiving logic device configured to communicate with the receiver and configured to pass data to the receiver from a selected peripheral device which is selected from one of the at least one peripheral device; and

an individual bus coupled between the at least one peripheral device and the receiving logic device,

wherein the receiving logic device is configured as an OR gate.

Claim 4 (original): A data communication device according to claim 3, further comprising a logic device within the peripheral device for enabling and disabling receiving data.

Claim 5 (original): A data communication device according to claim 4, the logic device further comprising at least one of an AND gate, a comparator, and a multiplexor.

Claim 6 (original): A data communication device according to claim 5, wherein the AND gate is configured to be in communication with the OR gate.

Claim 7 (original): A data communication device according to claim 5, wherein the comparator is configured to enable the AND gate upon receipt of an appropriate address signal.

Claim 8 (original): A data communication device according to claim 5, wherein the comparator is configured to enable the multiplexor upon receipt of an appropriate address signal.

Claim 9 (cancelled).

Claim 10 (previously amended): A data communication technique for use between a bus interface and at least one peripheral device, the data communication technique comprising the steps of:

identifying a peripheral device for communication; wherein an address identifies the peripheral device for communication;

receiving, at a receiving logic device, data signals from each of the peripheral devices;

transmitting to a receiver in the bus interface, through logic operations in the receiving logic device, only the data signal received from the identified peripheral device; and

providing, to the receiving logic device, from all peripheral devices other than the identified peripheral device, a data signal that contains only logic zero; and wherein the receiving logic device is an OR gate.

Claim 11 (original): A data communication technique in accordance with claim 10 further comprising the steps of:

enabling an AND gate in the identified peripheral device during a read operation; and

disabling a receiving multiplexor in the identified peripheral device during a read operation.

Claim 12 (original): A data communication technique in accordance with claim 10 further comprising the steps of:

disabling an AND gate in the identified peripheral during a write operation; and

enabling a receiving multiplexor in the identified peripheral during a write operation.

Claim 13 (original): A data communication technique in accordance with claim 10 further comprising the step of:

transmitting to a central processing unit, from the receiver in the bus interface, the signal from the identified peripheral device.

Claim 14 (original): A data communication technique in accordance with claim 11 wherein the enabling and disabling steps during the read operation occur during a third instruction cycle.

Claim 15 (original): A data communication technique in accordance with claim 12 wherein the enabling and disabling steps during the write operation occur during cycle a first instruction cycle.

Claim 16 (cancelled)

Claim 17 (previously amended): A bus interface device for communicating with at least one peripheral device, the bus interface device comprising:

a transmitter in communication with a common bus configured to communicate with the at least one peripheral device;

a receiving logic device configured to receive a logic zero signal from each of the at least one peripheral device that is not selected, and configured to receive a data signal from one of the at least one peripheral device that is selected; wherein the signals are received via separate buses; and

a receiver configured to receive the data signal from the receiving logic device,

wherein the receiving logic device is an OR gate.

Claim 18 (previously amended): The bus interface device according to claim 17, wherein the bus interface device is connected to a peripheral logic device within the at least one peripheral device for controlling the sending of data to the peripheral and the receiving of data from the peripheral.

Claim 19 (original): The bus interface device according to claim 18, the peripheral logic device further comprising at least one of an AND gate, a comparator, and a multiplexor.

Claim 20 (original): The bus interface device according to claim 19, wherein the OR gate is configured to be in communication with the AND gate in each of the at least one peripheral device using an individual bus line.

Claim 21 (original): The bus interface device according to claim 19, wherein the comparator is configured to enable the AND gate upon receipt of an appropriate address signal.

Claim 22 (original): The bus interface device according to claim 19, wherein the comparator is configured to enable the multiplexor upon receipt of an appropriate address signal.

Claim 23 and 24 (cancelled).